1. A method for addressing a display medium, the method comprising the steps of:

providing a plurality of voltage sources each having a different voltage level;

receiving a display signal indicating an addressing impulse to be applied to a pixel electrode;

selecting, responsive to the display signal, a portion of the plurality of voltage sources; and

connecting the selected voltage sources to a switch circuit that is connected to the pixel electrode.

2. The method of claim 1, wherein the step of connecting the selected voltage sources comprises simultaneously connecting the selected voltage sources to the switch circuit.

3. The method of claim 1, wherein the step of connecting the selected voltage sources comprises sequentially connecting the selected voltage sources to the pixel unit.

4. The method of claim 1, further comprising the step of activating the switch circuit to connect the selected voltage sources to the pixel electrode.

5. The method of claim 4, wherein the switch circuit comprises a transistor, and the step of activating the switch circuit comprises applying a selection voltage to a gate of the transistor.

6. The method of claim 1, wherein the display signal comprises a voltage magnitude number having digits that are associated with different ones of the plurality of voltage levels, and the step of selecting the portion of the plurality of voltage sources comprises selecting those of the plurality of voltage sources that are indicated for selection by the digits of the number.

7. The method of claim 6, wherein the voltage magnitude number is a binary number, and the step of selecting the portion of the plurality of voltage sources further comprises selecting those of the plurality of voltage sources that are indicated for

selection by the digits of the binary number that have a value of 1.

8. The method of claim 6, wherein the voltage magnitude number is a binary number, and the step of selecting the portion of the plurality of voltage sources further comprises selecting those of the plurality of voltage sources that are indicated for selection by the digits of the binary number that have a value of 0.

9. The method of claim 6, wherein each of the digits of the voltage magnitude number is associated with one of a plurality of sub-cycles of an addressing cycle, and the step of connecting the selected voltage sources comprises connecting each of the selected voltage sources during the associated sub-cycle.

10. The method of 1, wherein the display signal indicates a sequence of addressing impulses associated with a sequence of addressing cycles of the display, and wherein the steps of selecting the portion of the plurality of voltage sources and connecting the selected voltage sources are repeated for each of the sequence of addressing impulses.

11. The method of 1, wherein the step of selecting the portion of the plurality of voltage sources comprises selecting none of the plurality of voltage sources.

12. The method of 1, wherein the plurality of voltage levels have fixed voltage amplitude values.

13. The method of claim 1, wherein the display signal indicates a sequence of addressing impulses to be applied to a plurality of pixel electrodes during one addressing cycle of the display.

14. The method of claim 13, wherein the step of connecting the selected voltage sources to the switch circuit comprises connecting the selected voltage sources to a column electrode connected to a plurality of switch circuits that are each connected to a different one of the plurality of pixel electrodes.

15. The method of claim 14, further comprising the step of activating one of the plurality of switch circuits to connect the selected voltage sources to an associated one of the plurality of the pixel electrodes associated with the

addressing impulse.

16. The method of claim 1, further comprising storing data that identifies a present optical state of a portion of the display medium defined by the pixel electrode, and wherein the step of selecting the portion of the plurality of voltage sources comprises comparing a new optical state associated with the addressing impulse to the present optical state.

17. A method for addressing a display medium, the method comprising the steps of:

providing a capacitive element to apply an addressing voltage to a portion of the display medium;

providing a voltage source having a voltage greater than the addressing voltage; and

charging the capacitive element with the voltage source until the capacitive element applies the addressing voltage.

18. The method of claim 17, wherein charging the capacitive element comprises charging the capacitive element during a sub-cycle of a plurality of sub-cycles of an address cycle to apply the addressing voltage to the display medium during subsequent sub-cycles of the address cycle.

19. The method of claim 17, wherein charging the capacitive element comprises charging the capacitive element during a sub-cycle of a plurality of sub-cycles of an address cycle to apply a portion of an addressing impulse to the display medium during the sub-cycle.

20. The method of claim 17, wherein charging the capacitive element comprises connecting the voltage source to the capacitive element via a resistive circuit to mediate a rate of charging of the capacitive element.

21. The method of claim 20, wherein the resistive circuit comprises a transistor, and wherein the step of charging the capacitive element further comprises connecting the voltage source to the capacitive element via the transistor when a selection signal is applied to the transistor.

22. The method of claim 20, further comprising selecting a resistance of the resistive circuit and a capacitance of the capacitive element to control the charging rate of the capacitive element.

23. The method of claim 17, wherein the capacitive element comprises a pixel electrode.

24. An addressing structure for addressing a display medium, the structure comprising:

a pixel electrode;

a switch circuit connected to the pixel electrode;

a plurality of voltage sources each having a different voltage level; and

a switch unit configured to connect a portion of the plurality of voltage sources to the switch circuit responsive to a display signal indicating an addressing impulse.

25. The structure of claim 24, further comprising a voltage selector that selects the portion of the plurality of voltage sources.

26. The structure of claim 25, further comprising a data storage unit for storage of data that identifies a present optical state of a portion of the display medium defined by the pixel electrode, wherein the voltage selector selects the portion of the plurality of voltage sources in response to a comparison of the present optical state to a new optical state associated with the addressing impulse.

27. The structure of claim 24, further comprising a plurality of pixel electrodes, a plurality of switch circuits each connected to a different one of the plurality of pixel electrodes, and a column electrode connected to the plurality of switch circuits.

28. The structure of claim 27, further comprising a voltage selector configured to cause the switch unit to connect the selected voltage sources to the column electrode responsive to the display signal.

29. The structure of claim 28, wherein the voltage selector and the switch unit are included in a single component of the addressing structure.

30. The structure of claim 27, further comprising a selection signal generator configured to apply a selection signal to one of the plurality of pixel electrodes when connecting the column electrode to the selected voltage sources associated with the one of the plurality of pixel electrodes.

31. The structure of claim 24, further comprising a display signal generator configured to generate the display signal.

32. The structure of claim 24, wherein the switch unit comprises a plurality of transistors associated with the plurality of voltage sources.

33. An addressing structure for addressing a display medium, the structure comprising:

a voltage source;

a capacitive element to apply a voltage to a display medium defined by a pixel electrode;

a resistive switch configured to connect the voltage source to the capacitive element; and

an addressing voltage controller configured to turn the resistive switch on for a period of time to gradually charge the capacitive element until the capacitive element applies an addressing voltage that is less than a voltage level of the voltage source at the end of the period of time.

34. The structure of claim 33, wherein the period of time is associated with at least one sub-cycle of a plurality of sub-cycles of an addressing cycle, and the addressing voltage controller is configured to select the at least one sub-cycle in response to an addressing signal.

35. The structure of claim 34, wherein the period of time is associated with a portion of one sub-cycle of a plurality of sub-cycles of the addressing cycle, and the

addressing voltage controller is configured to select the portion of one sub-cycle in response to an addressing signal.

36. The structure of claim 33, wherein the resistive switch comprises a transistor.

37. The structure of claim 33, wherein the addressing voltage controller comprises a pulse width modulator.